CLAIMS

1. A cellular trench-gate transistor (1) comprising a silicon semiconductor body (10) having an array of transistor cells (TC), the cells being bounded by a pattern of array trenches (20) lined with insulating material (31,32,33) within the array, the array trenches (20) extending from an upper surface (10a) of the semiconductor body through a channel accommodating body region (23) into an underlying drain drift region (12), the insulating material in each array trench providing a thin gate dielectric insulating layer (31A) on a trench sidewall adjacent the channel accommodating body region (23) and a thick insulating layer (31B, 32,33) on a trench sidewall adjacent the drain drift region (12), conductive material in each array trench providing a gate electrode (41) on the thin trench sidewall insulating layer (31A) and a field plate (42) on the thick trench sidewall insulating layer (31B,32,33), wherein an integral first layer of silicon dioxide (31) extends from the upper surface (10a) of the semiconductor body (10) over top corners of each array trench (20), the integral first layer also providing the thin gate dielectric insulating layer (31A) and the integral first layer also providing a first part (31B) of a stack of materials which constitute the thick trench sidewall insulating layer (31B,32,33), a layer of silicon nitride (32) providing a second part of the stack, and a second layer of silicon dioxide (33) providing a third part of the stack.

2. A transistor as claimed in claim 1, wherein an edge termination for the transistor includes a perimeter trench (20A) around the array of transistor cells (TC), wherein the stack of materials (31B,32,33) which constitutes the thick trench sidewall insulating layer in the array trenches (20) extends around a top corner of the perimeter trench (20A) and on to the upper surface (10a) of the semiconductor body, and wherein conductive material (42) on the stack in the perimeter trench (20A) extends around the top corner of the perimeter trench to provide an edge field plate (41E) for the transistor.

3. A method of manufacturing a cellular trench-gate transistor (1)

comprising a silicon semiconductor body (10) having an array of transistor cells (TC), the cells being bounded by a pattern of array trenches (20) lined with insulating material (31,32,33) within the array, the array trenches (20) extending from an upper surface (10a) of the semiconductor body through a channel accommodating body region (23) into an underlying drain drift region (12), the insulating material in each array trench providing a thin gate dielectric insulating layer (31A) on a trench sidewall adjacent the channel accommodating body region (23) and a thick insulating layer (31B,32,33) on a trench sidewall adjacent the drain drift region, conductive material in each array trench providing a gate electrode (41) on the thin trench sidewall insulating layer (31A) and a field plate (42) on the thick trench sidewall insulating layer (31B,32,33), wherein the method includes the steps of:

(a) providing a hardmask (21) on the upper surface (10a) of the semiconductor body (10), then forming the array trenches (20) by etching using the hardmask, and then removing the hardmask (21);

(b) providing an integral first layer of silicon dioxide (31) which extends on the upper surface (10a) of the semiconductor body, over the top corners of the array trenches (20), and over the sidewalls and the base of each of the array trenches (20), the first layer of silicon dioxide (31) providing the thin gate dielectric insulating layer (31A) in the manufactured transistor;

(c) providing a layer of silicon nitride (32) over the first layer of silicon dioxide (31) and then providing a second layer of silicon dioxide (33) over the silicon nitride layer (32);

(d) providing conductive material in each array trench to form the thin field plate (42);

(e) selectively etching the second silicon dioxide layer (33) and then the silicon nitride layer (32) above the thin field plates (42) such that the thick trench sidewall insulating layer has a stack of the first silicon dioxide layer (31B), the silicon nitride layer (32) and the second silicon dioxide layer (33); and then

(f) providing conductive material in each array trench to form the thick gate electrode (41).

4. A method as claimed in claim 3, wherein the hardmask (21) used in step (a) is a single silicon dioxide layer.

5. A method as claimed in claim 3 or claim 4, including the further step of:

(g) forming layers for the channel accommodating body region (23) and source regions (24) for the transistor cells through the first layer of silicon dioxide (31) on the upper surface (10a) of the semiconductor body.

6. A method as claimed in any one of claims 3, 4 or 5, wherein steps for forming an edge termination for the transistor include:

(h) forming a perimeter trench (20A) around the array of transistor cells (TC) during step (a) and using the same hardmask (21);

(i) providing the first layer of silicon dioxide (31), the layer of silicon nitride (32) and second layer of silicon dioxide (33) around a top corner of the perimeter trench (20A) and on to the upper surface (10a) at the edge of the semiconductor body during steps (b) and (c);

(j) providing conductive material (42) in the perimeter trench (20A) by means of step (d);

(k) allowing the stack of the first silicon dioxide layer (31B), the silicon nitride layer (32) and the second silicon dioxide layer (33) to remain around a top corner of the perimeter trench (20A) and on the upper surface (10a) at the edge of the semiconductor body during the selective etching of step (e); and

(l) providing conductive material on the stack (31E,32E,33E) around the top corner of the perimeter trench (20A) to provide an edge field plate (41E) for the transistor at the same time as forming the thick gate electrode (41) in the array trenches (20) during step (f).

7. A transistor as claimed in claim 1 or claim 2, or a transistor manufactured by the method as claimed in any one of claims 3 to 6, wherein

the drain drift region (12) is more highly doped near the base of the array trenches (20) than near the channel accommodating body region (23).

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